2021

(July)

COMPUTER APPLICATION

(Honours)

(Computer System Architecture)

(BCA–203)

Marks : 75

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer **one** question from each Unit

UNIT—I

1. *(a)* With the help of a block diagram, explain the functional units of a computer system. 4+2=6

(b) Explain the purpose of the following registers (any *three*) : 3×3=9

(i) Instruction Register (IR)

(ii) Program Counter (PC)

(iii) Memory Data Register (MDR)

(iv) Memory Address Register (MAR)

(v) Accumulator (AC)

2. *(a)* Write down a program to evaluate the following using a general purpose registers with two address instructions : 6

A B*[C*D E*(F G)]

(b) What is an addressing mode? Describe indirect and immediate addressing modes. 3+3+3=9

UNIT—II

3. *(a)* Describe the steps by which a single computer instruction is executed with the help of microprogram routines. 9

(b) What is mapping with respect to address sequencing? Explain with an example. 2+4=6

4. *(a)* Define the following : 2×4=8

(i) Microoperation

(ii) Microinstruction

(iii) Microprogram

(iv) Microcode

(b) What is a microprogram sequencer? With block diagram, explain the working of microprogram sequencer. 2+5=7

UNIT—III

5. *(a)* What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each? 4+4=8

(b) What are interrupts? Explain the steps to handle interrupts using daisy-chaining method. 2+5=7

6. *(a)* Describe Direct Memory Access (DMA) with the help of a diagram. 9

(b) Design a parallel priority interrupt hardware for a system with eight interrupt sources. 6

UNIT—IV

7. *(a)* Briefly describe different techniques used for handling branching in an instruction pipeline. 10

(b) A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? 4+1=5

8. *(a)* Explain arithmetic pipeline with the help of a diagram. Discuss three major difficulties that cause the instruction pipeline to deviate from its normal operation. 4+6=10

(b) Describe how matrix multiplication can be performed in computers with vector processor. 5

UNIT—V

9. *(a)* With the help of a block diagram and function table, describe a RAM chip. 5+4=9

(b) Answer the following : 2×3=6

(i) How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(ii) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

(iii) How many lines must be decoded for chip select? Specify the size of the decoders.

10. *(a)* Explain virtual memory concept. Differentiate between virtual address and physical address. 4+4=8

(b) Explain cache memory. Define HIT, MISS and HIT ratio. 4+3=7

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